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In the Claims:

Please amend claims 1-21 as follows:

1. (Currently Amended) A semiconductor integrated circuit having at least one self-construction circuit, said self-construction circuit comprising:

storing means for reading data therefrom and writing data thereinto;

comparing means for providing a comparison result; and

variable address converting means for converting an address signal inputted to said self-construction circuit into a write address in the storing means for writing into the storing means input data of a hardware description language statement of a newly designated logical function based on the comparison result by the comparing means,

wherein said comparing means compare input data continuously supplied to said self-construction circuit with the input data written into and then read from the storing means, and

wherein the ~~input data is written to the storing means so that~~ data written into then read from the storing means is an ~~expected~~ output signal ~~according to~~ of the self-construction circuit according to the newly designated logical function with respect to an input signal of the self-construction circuit.

2. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 1, wherein a plurality of the storing means, a plurality of the comparing means, and a plurality of the variable address converting means are provided on a single semiconductor chip.

3. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 1, wherein the storing means include a volatile memory.

4. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 1, wherein the variable address converting means comprise:

a memory array in which a plurality of memory cells are arranged in a matrix shape;

an address decoder that selects the memory cells in the memory array based on an input address signal;

amplifying means for amplifying a signal read from the memory array; and

updating means for updating the input address signal based on a control signal.

5. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 4, wherein the memory array is a volatile memory.

6. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 1, 2, 3, 4, or 5, further comprising: data holding means for holding data read from the storing means; a switch matrix for switching the input address signal or an output signal of the data holding means and for supplying the switched signal to the variable address converting means and to the storing means, wherein the storing means store control information of each switch in the switch matrix.

7. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 6, wherein the data holding means comprise:

latching means for latching data read from the memory array; and

gate means for determining whether to latch the data by the latching means based on the data read from the memory array.

8. (Currently Amended) A method for constructing a logic integrated circuit, comprising:

providing at least one self-construction circuit capable of being converted to operating different logical functions as a building block for the logic integrated circuit;

assigning a desired logical function to said self-construction circuit by sending an address signal to the self-construction circuit;

self-decoding design data coded at logical function level of the desired logical function by the self-construction circuit;

self-converting by the self-construction circuit to ~~operate~~ provide an output signal according to the desired logical function with respect to an input signal thereof; and

self-verifying by the self-construction circuit to verify whether the output signal complies with the desired logical function with respect to the input signal.

9. (Currently Amended) The [[A]] method for constructing the logic integrated circuit according to claim 8, wherein control means for decoding the design data are formed on an identical ~~semi-conductor~~ semiconductor chip as the self-construction circuit.

10. (Currently Amended) The [[A]] method for constructing the logic integrated circuit according to claim 9, wherein a memory for storing the design data coded at logical function level is formed on an identical semiconductor chip as the control means and the self-construction circuit.

11. (Currently Amended) A semiconductor integrated circuit having at least one self-construction circuit, said self-construction circuit comprising:

storing means for storing information obtained from a description in which a newly assigned logical function is represented in a hardware description language and for obtaining an output signal according to the newly assigned logical function with respect to an input signal supplied to an address terminal thereof; and

means for verifying whether ~~a correlation between~~ the output signal ~~and the input signal complying~~ complies with the newly assigned logical function with respect to the input signal.

12. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 11, wherein the logical function includes a combinational logical function.

13. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 12, wherein the logical function includes a sequential logical function.

14. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 11, wherein the storing means are read- and write-enable storing means.

15. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 11, wherein the means for verifying includes converting means for converting into the

information written to the storing means from the description represented in the hardware description language.

16. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 15, wherein the storing means stores the description represented in the hardware description language.

17. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 2, wherein the storing means are a volatile memory.

18. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 2, wherein the variable address converting means comprise:

a memory array in which a plurality of memory cells are arranged in a matrix shape;

an address decoder that selects the memory cells in the memory array based on an input address signal;

amplifying means for amplifying a signal read from the memory array; and

updating means for updating the input address signal based on a control signal.

19. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 3, wherein the variable address converting means comprise:

a memory array in which a plurality of memory cells are arranged in a matrix shape;

an address decoder that selects the memory cells in the memory array based on an input address signal;

amplifying means for amplifying a signal read from the memory array; and

updating means for updating the input address signal based on a control signal.

20. (Currently Amended) The [[A]] semiconductor integrated circuit according to claim 4, wherein the variable address converting means comprise:

a memory array in which a plurality of memory cells are arranged in a matrix shape;

an address decoder that selects the memory cells in the memory array based on an input address signal;

amplifying means for amplifying a signal read from the memory array; and

updating means for updating the input address signal based on a control signal.

21. (Currently Amended) The [[A]] method for constructing the logic integrated circuit according to claim 8, wherein the self-decoding, self-converting, and self-verifying steps ~~by said self-construction circuit~~ involves:

converting the address signal inputted into a write address;

comparing input data continuously supplied to said self-construction circuit with the input data written into and then read from the self-construction circuit; and

writing into said self-construction circuit input data of the desired designated logical function into the write address based on a result determined in the comparing step.